WARM WELCOME to 1st SystemC Evolution Day!

• **Review:** DVCon Europe Nov 2015
  – SystemC BoF 90min
  – Great interest, but a bit short...

• **Idea born** (at DVCon debrief)
  – Lean, full day workshop
  – Focus on technical discussions
WARM WELCOME to 1st SystemC Evolution Day!

• Today
  – SCED is real, with full program
    • 60+ registrations
    • 21 companies, 7 universities
  – Let’s have good discussions and insights for evolving SystemC

• Next
  – Follow-up in Working Groups
  – DVCon Europe 2016, Oct 19th-20th
    • SystemC remains a focus area
Event Sponsor

Accellera Global Sponsors

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Special Thanks*

• **Organization Team**
  – Oliver Bell, Philipp Hartmann, Intel
  – Martin Barnasconi, NXP
  – Matthias Bauer, Infineon

• **Logistics and Organization**
  – Lynn Bannister-Garibaldi, Accellera
  – Anja Holweg, Intel

• **Moderators**
  – Ralph Görgen, OFFIS
  – Martin Schnieringer, Bosch
  – Mark Burton, GreenSocs
  – Martin Barnasconi, NXP

• **Presenters**
  – Domenik Strasser, OneSpin
  – Rainer Doemer, UC Irvine
  – Jakob Engblom, Intel
  – Karsten Einwich, COSEDA

* In order of appearance
## Morning program

<table>
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<th>Time</th>
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<td>10:15 – 10:45</td>
<td>Welcome, Introduction, SystemC WG Updates</td>
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|          | • Addressing the HLS Coding Barrier  
|          |     *Dominik Strasser, OneSpin solutions*  |
|          | • Seven Obstacles in the Way of Parallel SystemC Simulation  
|          |     *Rainer Doemer, UC Irvine*  |
|          | • Events and Timing in TLM – Extend and Clarify  
|          |     *Jakob Engblom, Intel Corp.*  |
|          | • Tracing and Interactive Test/Debug in SystemC and SystemC AMS  
|          |     *Karsten Einwich, COSEDA*  |
| 12:45 – 13:45 | Lunch break – sponsored by Accellera |
# Afternoon program

<table>
<thead>
<tr>
<th>Time</th>
<th>Room 02.1.110 (here)</th>
<th>Room 02.1.160</th>
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</thead>
<tbody>
<tr>
<td>13:45 – 15:15</td>
<td><strong>#1.1 SystemC/TLM and Language Standards (C++11/14)</strong>&lt;br&gt; <em>Ralph Görgen, OFFIS</em></td>
<td><strong>#2.1 TLM Standard for Serial Interfaces</strong>&lt;br&gt; <em>Martin Schnieringer, Bosch</em></td>
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<td>15:15 – 15:45</td>
<td><strong>Coffee break</strong> – sponsored by Accellera</td>
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<tr>
<td>15:45 – 17:15</td>
<td><strong>#1.2 Multi-Threaded SystemC and External Interfaces</strong>&lt;br&gt; <em>Mark Burton, GreenSocs</em></td>
<td><strong>#2.2 UVM-SystemC &amp; Config., Control and Inspection (CCI)</strong>&lt;br&gt; <em>Martin Barnasconi, NXP</em></td>
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<td>17:15 – 17:45</td>
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<tr>
<td>17:45 – 18:30</td>
<td><strong>Wrap-up, Next Steps, Closing</strong></td>
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<tr>
<td>19:30 – 21:30</td>
<td><strong>Dinner</strong> – (not included, self-paid)</td>
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Results collection

• In the **Technical Sessions**, please
  – nominate a **secretary to take minutes**
  – prepare **summary** on 1-2 slides for wrap-up session
    • Main consensual/controversial points
    • Next steps in Accellera (including owners and destination WGs)

• Detailed results will be forwarded to Accellera WGs
  – Including presented material
  – **Join Accellera WGs** to continue your participation!
Dinner

• Taj am Campeon – [http://www.taj-am-campeon.de](http://www.taj-am-campeon.de)
• 19:30 – 21:30
• Building 10 – here on campus

• Please announce your participation until 11:00!
• *(Food/drinks not included – self-paid)*
SystemC WG Updates
Accellera SystemC Working Groups

- **Language** Working Group (LWG)
  - Chairs: Philipp A. Hartmann (Intel), Andy Goodrich (Cadence)

- **Transaction-Level Modeling** Working Group (TLMWG)
  - Chair: Bart Vanthournout (Synopsys)

- **Analog/Mixed-Signal** WG (AMSWG)
  - Chairs: Martin Barnasconi (NXP), Christoph Grimm (TU Kaiserslautern)

- **Configuration, Control & Inspection** WG (CCIWG)
  - Chairs: Trevor Wieman (Intel), Bart Vanthournout (Synopsys)

- **Synthesis** Working Group (SWG)
  - Chairs: Andres Takach (Mentor), Mike Meredith (Cadence)

- **Verification** Working Group (VWG)
  - Chairs: Stephan Schulz (Fraunhofer), Bas Arts (NXP)
SystemC Language Working Group

• **Charter:** Responsible for the definition and development of the **SystemC core language**, the foundation on which all other SystemC libraries and functionality are built.

• **Current status**
  – Currently collecting, addressing, refining proposals and errata towards IEEE 1666-201x
  – Adding extensions to the core language (e.g. as needed by other SystemC-related WGs)

• **Plans for 2016**
  – Preparing an intermediate **2.3.2 release** for public review
SystemC TLM Working Group

• **Charter:** The Transaction-level Modeling Working Group (TLMWG) is responsible for the definition and development of methodology and add-on libraries for transaction-level modeling in SystemC.

• **Current status**
  – Accellera TLM-2.0 became part of IEEE 1666-2011, PoC implementation 2.0.3 bundled with SystemC 2.3.1

• **Plans for 2016**
  – Working on TLM interfaces, extensions, and guidelines to improve modeling of protocols beyond memory-mapped I/O
  – „TLM signals“; serial, bi-directional communication, ...
SystemC Analog/Mixed-Signal WG

- **Charter:** The SystemC AMSWG is responsible for the standardization of the SystemC AMS extensions, defining and developing the language, methodology and class libraries for analog, mixed-signal and RF modeling in SystemC.

- **Current status**
  - IEEE 1666.1-2016 SystemC AMS released by IEEE-SA
    - New features under development (e.g. piece-wise-linear modeling, tracing customization, analog solver parameters)

- **Plans for 2016**
  - Publish User’s Guide update based on SystemC AMS 2.0
• **Charter:** Responsible for standards that allow **tools to interact with models** in order to perform activities such as setup, debug, and analysis.

• **Current status (Configuration)**
  – Initial Proof-of-Concept with usage examples
  – Focus on key improvements and LRM

• **Plans for 2016**
  – Resourced plan in place to finalize draft Configuration standard for public review
SystemC Synthesis WG

- **Charter:** To define the SystemC synthesis subset to allow synthesis of digital hardware from high-level specifications.

- **Current status**
  - SystemC Synthesizable Subset approved by Accellera board (Q1 2016)
    
    http://workspace.accellera.org/apps/org/workgroup/swg

- **Plans for 2016**
  - Starting work on impact of C++11/14 and synthesizable HLS.
    - Working document SWG_SystemC_Extensions.docx
  - Anticipate that this will force closer collaboration with LWG.
SystemC Verification WG

• **Charter:** The VWG is responsible for defining verification extensions to the SystemC language standard, and to enrich the SystemC reference implementation by offering an add-on libraries to ease the deployment of a verification methodology based on SystemC.

• **Current Status**
  – Released version 2.0 of SystemC Verification library in April 2014
  – Released version alpha1 of UVM-SystemC (LRM/PoC) in December 2015

• **Plans for 2016**
  – Integration of CRAVE into UVM-SystemC (tutorial abstract submitted to DVCon Europe 2016)
  – Standardization of coverage APIs (coverage groups, bins, etc.)
  – Further explorations of needs regarding SystemC/TLM
Accellera Systems Initiative
IP Rights Policy Slides

For information contact ipr-chair@lists.accellera.org
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• Early identification of holders of potential Essential Patent Claims is strongly encouraged
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This slide set is available at:
http://www.accellera.org/about/policies/accellera_systems_initiative_IPR_slides.pdf
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