Generic Payload Enhancement

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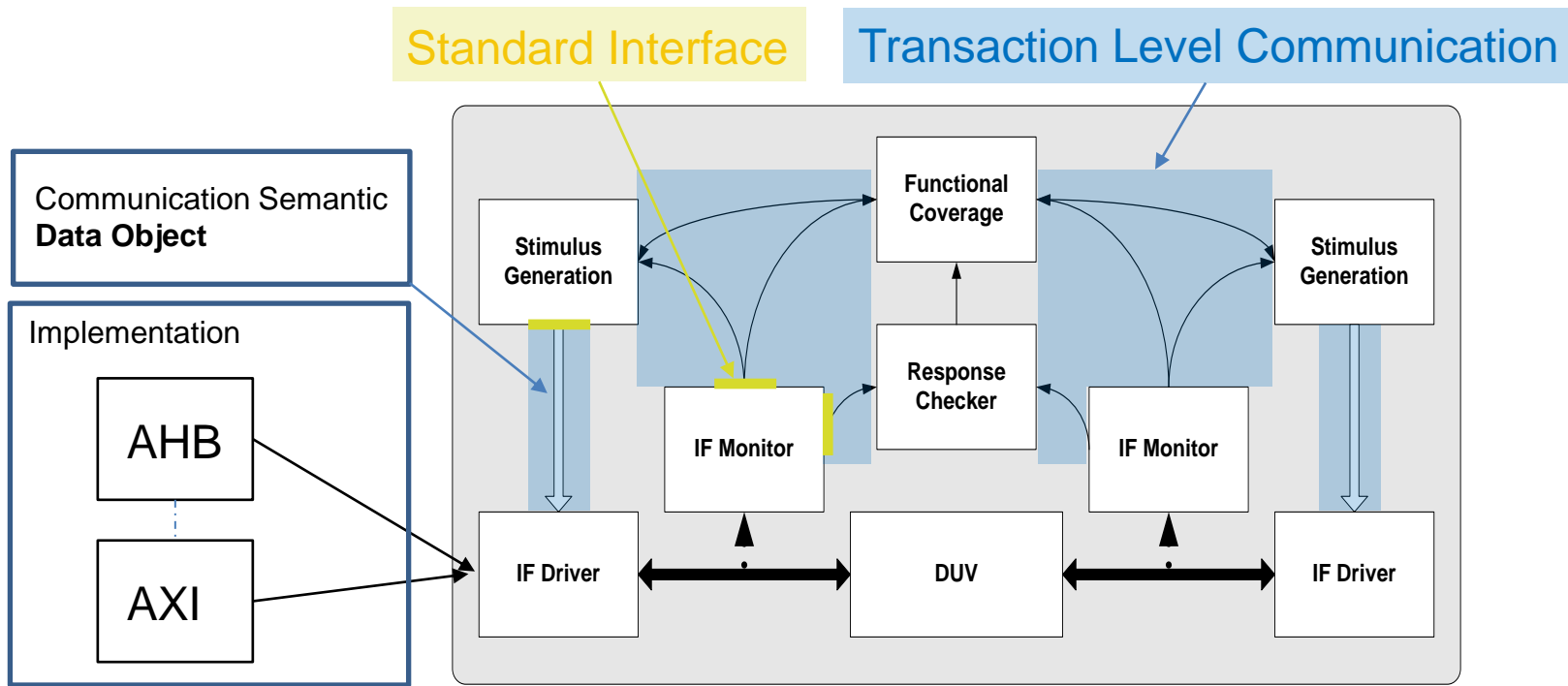
Agenda

- Introduction
- Proposals
  - "Mode" Support
  - Resource Protection
- Discussion

Introduction - Background

Problem: Interoperability between components and used generic payload
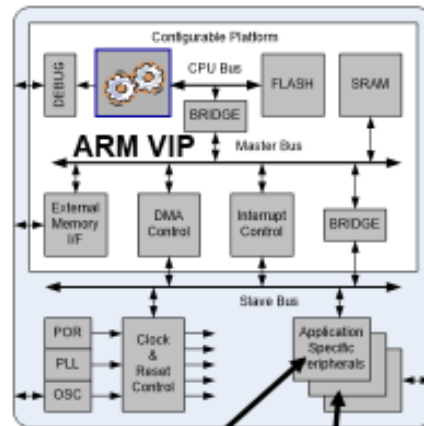
Testbench Infrastructure Overview
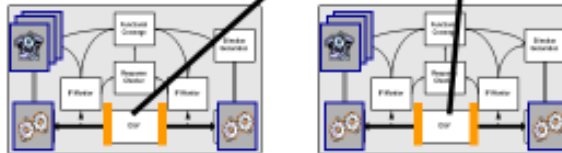
Introduction - Background

Testbench Reuse

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Reuse of Verification Work

Launched by Motorola
freescale semiconductor

ARM VIP

From Module to SoC Level

- Reuse of test bench
  - Address mapping
  - Interrupt mapping
  - Pin driver multiplexing
  - Bus driver mapping

- ARM bus driver replaces module bus driver

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Introduction – Data Object

Data object content was defined by

- Register Properties
  - Register Address
  - Register Size
  - Register Mode Properties

| Bus Master | → | Design Register |

Mode examples

- User
- Supervisor
- Debug
- Test

Table 2.1. ARM processor modes

Processor mode	Architectures	Mode number
User	All	0b10000
FIQ - Fast Interrupt Request	All	0b10001
IRQ - Interrupt Request	All	0b10010
Supervisor	All	0b10011
Abort	All	0b10111
Undefined	All	0b11011
System	ARMv4 and above	0b11111
Monitor	Security Extensions only	0b10110

http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.dui0204j/Chdddhea.html

Proposal "Mode" Support

Proposal is about adding a data field to the GP class or class extension that allows to carry "mode" information. The name and the symbolic name definition of the modes are to be defined by the community.

SVBCL RegisterCmd	UVM GP	Comment
cmd	m_command	
addr	m_address	
size	m_length	
	m_byte_en	
data	m_data	
mode		Missing Information
ack	m_response_status	
endian		Handled by m_byte_en

- Advantage is that no custom extension is required

Example:
```
enum m_mode_e {not_defined=0, user=1,
test=2}

m_mode_e m_mode;
```
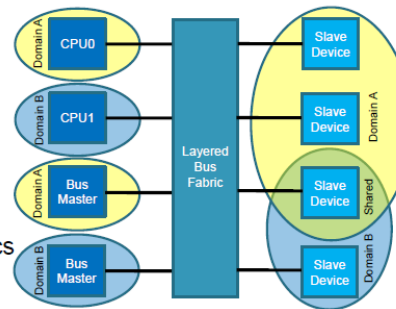
GP Generic Payload

Proposal Resource Protection

Proposal is about adding a data field to the GP class or class extension that allows to carry a master ID information. The name definition of the field are to be defined by the community

Resource Domains

· Use **resource domains** to partition the system
  - Masters are assigned to a resource domain
  - Slave access permissions are defined per resource domain
  - Memory region access permissions are defined per resource domain
· Sideband signals of bus fabrics carry resource domain ID

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https://www.google.com/search?q=resource+domain+controller&ie=utf-8&oe=utf-8&client=firefox-b-ab

- Advantage is that no custom extension is required

Example: `int m_id; // -1 means did not used`

Discussion