WELCOME TO THE

4TH EDITION

EVOLUTION DAY

OCT 31, 2019 | MUNICH | GERMANY

accellera SYSTEMS INITIATIVE

SYSTEMC™ EVOLUTION DAY
OCT 31, 2019 | MUNICH | GERMANY

WARM WELCOME to 4th SystemC Evolution Day!

- 2nd time co-located with DVCon Europe @ Holiday Inn
- Let's have good discussions and insights for further evolving SystemC!
  - unique opportunity to exchange, learn from peers and contribute to SystemC
- If you are a system-level modeling enthusiast, expert or beginner
  - thanks for spending Halloween with us!
- All Slides will be made available at Accellera page: https://www.accellera.org/news/events/systemc-evolution-day-2019

accellera SYSTEMS INITIATIVE

SYSTEMC™ 2 EVOLUTION DAY
OCT 31, 2019 | MUNICH | GERMANY

Goals and objectives

- Evolution of SystemC standards to advance the SystemC ecosystem
- Discuss current and future standardization topics around SystemC
- Identify opportunities to enable (accelerated) inclusion in Accellera and/or IEEE SystemC standards
- Capture ideas and discussions and bring them to the associated SystemC WG for further consideration

Thanks to our Event Sponsors

cadence®

Mentor® A Siemens Business

SYNOPSYS®

accellera SYSTEMS INITIATIVE™

Special Thanks

- **SystemC Evolution Day Organization Team**
  - Oliver Bell, Intel (Chair)
  - Martin Barnasconi, NXP
  - Andrew Stevens, Infineon
  - Ola Dahl, Ericsson
  - Philipp A. Hartmann, Intel
  - Volkan Esen, Infineon
  - Ingo Feldner, Bosch
  - Tran Nguyen, ARM
  - Manfred Thanner, NXP
  - Jerome Cornet, ST
- **Today's SystemC WG representatives (+ making notes)**
  - Philipp A. Hartmann: LWG
  - Martin Barnasconi: AMS, VWG, (MLVWG)
  - Bart Vanthournout: TLM WG, CCI WG
  - Rauf Salimi: Synthesis, new requests

Meeting summary and actions

- Meeting summary and actions will be forwarded to Accellera WGs
- Today‘s SystemC WG representatives will make notes and will bring the discussion to the associated WG
- Today‘s presented material will be stored in the Accellera WG workspace as reference and further discussion
- **Join Accellera WGs** to continue your participation!

Morning program

08:30 – 09:00	**Welcome coffee** – hosted by Accellera
09:00 – 09:30	**Introduction and SystemC Working Groups standardization update**
09:30 – 10:15	**SystemC and Digital Twin: Good match or Not?** *Martin Barnasconi, NXP*
10:15 – 10:45	**Coffee break** – hosted by Accellera
10:45 –12:30	**Simulation, Kernel Technology, Tracing**
10:45-11:15	**Pushing the Limits of Standard-Compliant Parallel SystemC Simulation** *Rainer Doemer, University of California, Irvine*
11:15-12:00	**Synchronizing simulators, and Save and Restore** *Mark Burton, GreenSocs*
12.00-12:30	**Improving the Usability and Performance of Tracing in SystemC** *Rauf Salimi, Philipp Hartmann, Intel*
12:30 13:45	**Lunch break** – courtesy of Accellera, Cadence, Mentor a Siemens Business, and Synopsys

Afternoon program

13:45- 15:00	**TLM, Interoperability, Metrics**
13:45-14:10	**Methodology for defining bus specific Programmer's View extensions to TLM2.0** *Umesh Sisodia, Prince Arora, CircuitSutra Technologies Pvt Ltd*
14:10-14:35	**Follow up on GP extension standard, Clock and Reset SC standard** *Joachim Geishauser, NXP*
14:35-15:00	**SystemC Modeling Metrics** *Ingo Feldner, Tim Kraus, Bosch*
15:00 - 15:30	**Coffee break** – hosted by Accellera
15:30-17:00	**Model Creation, High Level Synthesis**
15:30-16:15	**Re-envisioning CCI inspection** *Bill Bunton, Philipp Hartmann, Intel; Michael Lebert, Ola Dahl, Ericsson*
16:15-17:00	**Advanced assertion checking in SystemC High-Level Synthesis flows** *Bob Condon, Intel*
17:00-17:30	**Wrap-up & Closing**

Welcome @ Holiday Inn

Coffee Foyer

08:30-09:00
10:15-10:45
15:00-15:30

Lunch Restaurant

12:30-13:45

For good discussions – coffee and food is available ☺

Internet: DVCon2019 (SSID+pwd)

accellera SYSTEMS INITIATIVE

SYSTEMC EVOLUTION DAY
OCT 31, 2019 | MUNICH | GERMANY

For more information contact ipr-chair@lists.accellera.org

ACCELLERA SYSTEMS INITIATIVE IP RIGHTS POLICY SLIDES

Accellera IP Rights Fundamentals

- All participants in an Accellera WG meeting must abide by the Accellera IP Rights Policy which can be found at www.accellera.org/about/policies/
- The Accellera Board and its committees operate in an open manner. To that end, no material submitted to the Accellera Board or its committees will be accepted or considered if it contains any statement that places any burden on the recipient(s) with respect to confidentiality or copyright. Any communication or other collateral material, including electronic mail, containing language with such restrictive wording will not be accepted or considered.
- Slide presentations at any Accellera meeting containing a copyright notice(s) from the presenter's employer or a company that the presenter represents will be accepted only if a duly filled-in copyright permission template slide is the first slide (after the title slide) in the presentation.

Participants, Patents, and Duty to Inform

All participants in this meeting have certain obligations under Accellera's IP Rights Policy

Participants:

- Shall inform Accellera (or cause Accellera to be informed) of the identity of each holder of any potential Essential Patent Claims of which they are personally aware if the claims are owned or controlled by the participant or the entity the participant is from, employed by, or otherwise represents
  - "Personal awareness" means that the participant is personally aware that the holder may have a potential Essential Patent Claim, even if the participant is not personally aware of the specific patents or patent claims
- Should inform Accellera (or cause Accellera to be informed) of the identity of any other holders of such potential Essential Patent Claims (that is, third parties that are not affiliated with the participant, with the participant's employer, or with anyone else that the participant is from or otherwise represents)
- The above does not apply if the patent claim is already the subject of an Accepted Letter of Assurance that applies to the proposed standard(s) under consideration by this group
- Early identification of holders of potential Essential Patent Claims is strongly encouraged
- No duty to perform a patent search

IPR and Patent-Related Documents

- All participants should be familiar with their obligations under the Accellera IP Rights Policy, including the antitrust and competition law guidelines. The IP Rights Policy and related documents are available at:

  http://www.accellera.org/about/policies/

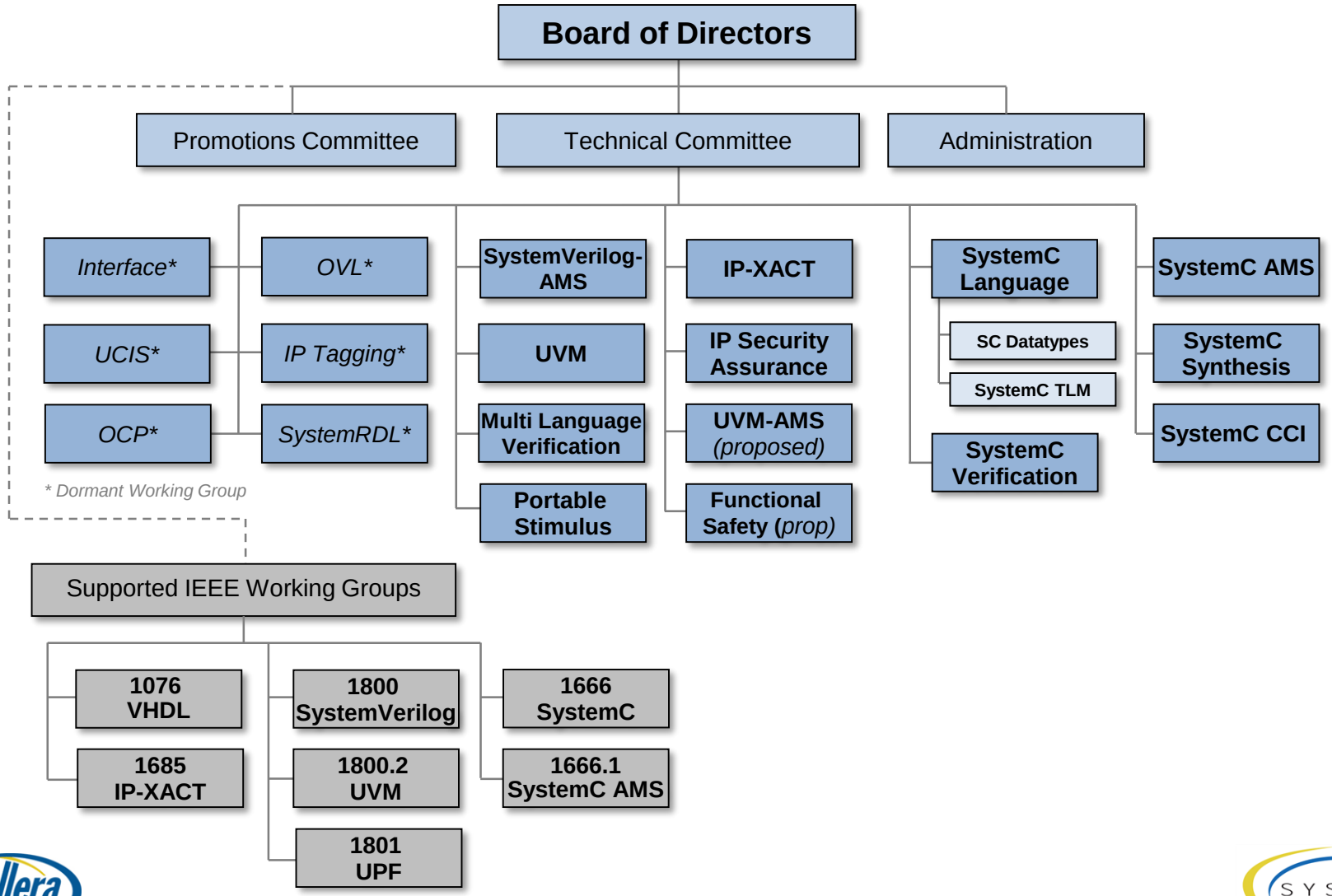
If you have questions, contact the Accellera Systems Initiative IP Rights Committee Administrator at ipr-chair@lists.accellera.org or visit www.accellera.org

This slide set is available at:
http://www.accellera.org/about/policies/accellera_systems_initiative_IPR_slides.pdf

SYSTEMC WORKING GROUP UPDATE

Martin Barnasconi, Accellera Technical Committee Chair

Accellera Systems Initiative



Accellera SystemC Working Groups

- **Language** Working Group (LWG)
  - Chairs: Philipp A. Hartmann (Intel), Vice-chair: Andy Goodrich (Allied member)
- **Transaction-Level Modeling** Working Group (TLMWG)
  - Chair: Bart Vanthournout (Synopsys)
- **Analog/Mixed-Signal** Working Group (AMSWG)
  - Chair: Martin Barnasconi (NXP), Vice-chair: Christoph Grimm (TU Kaiserslautern)
- **Configuration, Control & Inspection** Working Group (CCIWG)
  - Chairs: Trevor Wieman (Intel), Vice-chair: Bart Vanthournout (Synopsys)
- **Synthesis** Working Group (SWG)
  - Chairs: Andres Takach (Mentor), Vice-chair: Mike Meredith (Cadence)
- **Datatypes** Working Group (SDTWG)
  - *Acting chair: Mark Johnstone (NXP)*
- **Verification** Working Group (VWG)
  - Chairs: Stephan Schulz (Bosch), Vice-chair: Bas Arts (NXP)

IEEE related Working Groups

- **P1666 (SystemC)**
  - IEEE Standard for Standard SystemC Language Reference Manual Working Group (LWG)
  - Latest version: IEEE 1666-2011, published 2012-01-09
  - Chair: Jerome Cornet (ST Microelectronics)
  - Status: P1666 WG active, working on next revision of 1666
- **P1666.1 (SystemC AMS)**
  - IEEE Standard for Standard SystemC(R) Analog/Mixed-Signal Extensions Language Reference Manual
  - Latest version: IEEE 1666.1-2016, Published 2016-04-06
  - Chair: Martin Barnasconi (NXP)
  - Status: P1666.1 WG not active

SystemC WG's brief update

- SystemC AMS
  - User's Guide release to be released in December 2019
- SystemC Language
  - SystemC reference Implementation now publicly available on Github: https://github.com/accellera-official
  - Review and implement tickets for inclusions in IEEE P1666
  - *TLM and Datatypes sub-WGs inactive*
- SystemC CCI
  - Review started of checkpointing contribution of Intel
- SystemC Synthesis
  - Review use of C++11 language constructs for synthesis
  - Discussing boundaries for support for elaboration
- SystemC Verification
  - Finalizing UVM-SystemC 1.0beta3 including UBUS example