SystemC Evolution Fika – April 2022

Introduction

Ola Dahl, Ericsson

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SystemC Evolution Fika - 7 April 2022

Workshop on the Evolution of SystemC Standards

In 2022 we are continuing the SystemC Evolution by organizing a series of online workshops to discuss the latest SystemC developments and applications. We refer to these workshops as *fikas*, to honor the fika tradition of sharing a coffee, slowing down a bit, and talking about things that we care about.

Event information

Date: **7 April 2022**
Time: **16:00 - 18:00 CEST**
Location: Online, Virtual Workshop.

Registration

Registration is free of charge. Register here.

NOTE: After registration you will receive an email including meeting details to attend the online event.

Organization Team

- Ola Dahl, Ericsson (Chair)
- Martin Barnasconi, NXP
- Jerome Cornet, STMicroelectronics
- Christian Sauer, Cadence
- Mark Burton, GreenSocs
- Peter de Jager, Intel

https://systemc.org/events/scef202204/

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Agenda

Main theme of the event: Parallelization of SystemC simulations

Time (CEST)	Title	Presenter(s)	Affiliation(s)
16:00 - 16:10	**Introduction**	Ola Dahl	Ericsson, Stockholm, Sweden
16:10 - 16:30	**sc-during: Parallel Programming on Top of SystemC** Abstract	Matthieu Moy	Laboratoire d'Informatique du Parallélisme (LIP), Lyon, France
16:30 - 16:50	**Ensuring reproducible parallel LT TLM models simulation with SCale SystemC kernel** Abstract	Tanguy Sassolas	CEA - LIST, Gif-sur-Yvette, France
16:50 - 17:10	**The Intel Simics Simulator and SystemC and Threading** Abstract	Jakob Engblom	Intel, Stockholm, Sweden
17:10 - 17:30	**RISC: A Compiler for Parallel SystemC with Maximum Standard Compliance** Abstract	Rainer Dömer	University of California, Irvine, CA, USA
17:30 - 18:00	**Discussion**	All participants. Moderator: Ola Dahl	

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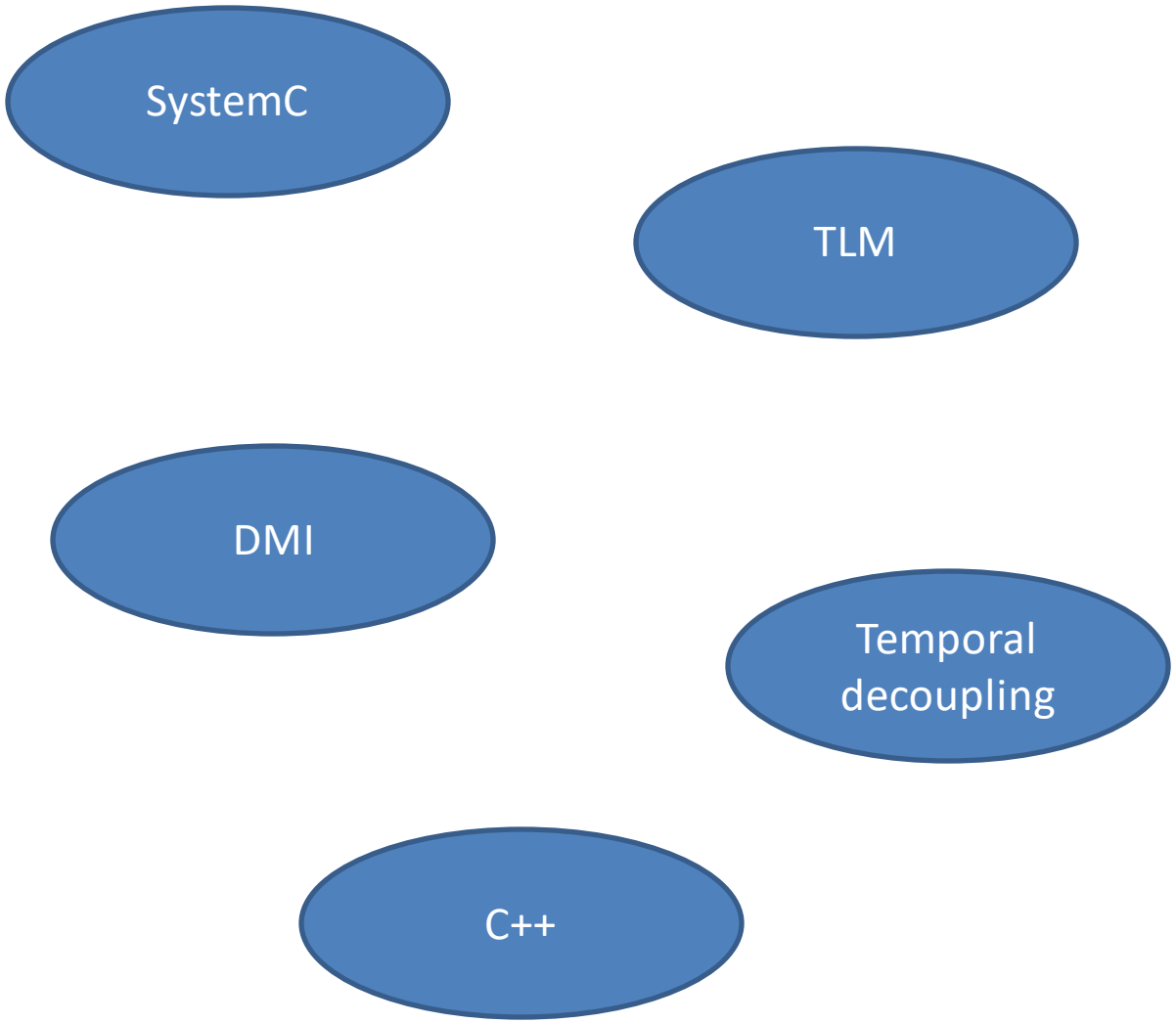

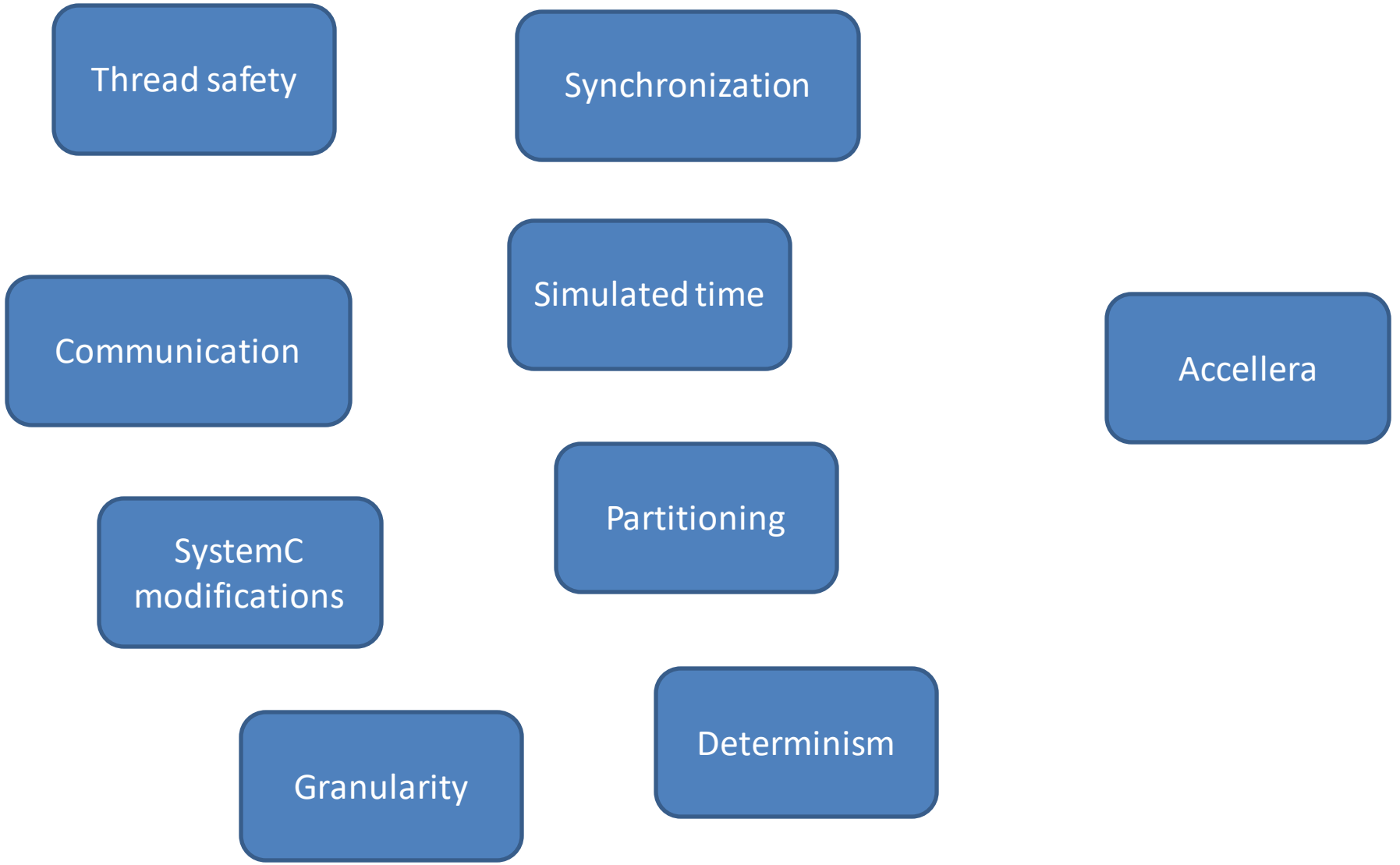

Safety-related Use Cases of Virtual Prototypes

- Increasingly, virtual prototypes are used in safety-related context. In automotive and avionics, for instance, commonly known and discussed use cases include the development of embedded software as well as their use as executable spec across the vendor chain
- We would like to look at their value for the design & verification of safety-critical systems
- How are they used? What are the benefits? How useful are the results?
- We are looking for contributions illustrating the use of Virtual Prototypes for
  - (what do we need?) the validation of safety relevant scenarios, interfacing, e.g. with requirement management, FME(D)A and modeling methodologies
  - (will it work?) the design and verification of safety mechanisms, potentially applying fault injection techniques to stimulate faulty behavior
  - (how well will it work? what can we predict?) the extraction of relevant metrics and their correlation to implementation, such as the fault space and its diagnostic coverage
- How well is this use supported by current SystemC standard and established modeling approaches?
- Please share your insights, observation and practical (good and/or bad) experience!

Discussion