SystemC Evolution Fika – 12 September 2023

Introduction

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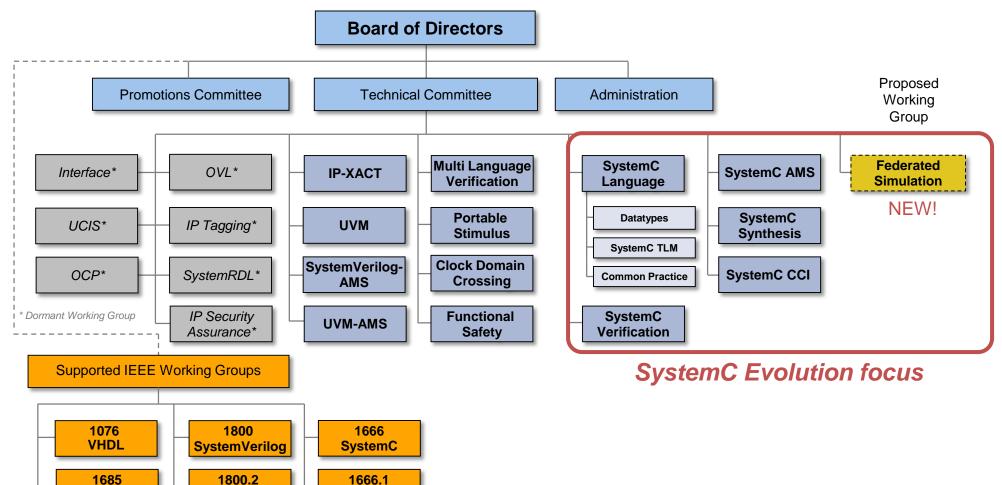
SystemC Evolution Fika - Agenda

Time (CEST)	Title	Presenter(s)	Affiliation(s)
16:00 - 16:10	Welcome & Introduction	Mark Burton ¹ , Martin Barnasconi ²	¹ Qualcomm, ² NXP
16:10 - 16:40	SystemC IEEE 1666 update	Jérôme Cornet	STMicroelectronics, IEEE P1666 Chair
16:40 - 17:10	Tracing in SystemC	Lukas Jünger ¹ , Eyck Jentzsch ² , Rocco Jonack ²	 ¹ MachineWare GmbH, ² MINRES Technologies
17:10 - 17:30	Q&A		





Accellera SystemC Working Groups





IP-XACT



SystemC AMS

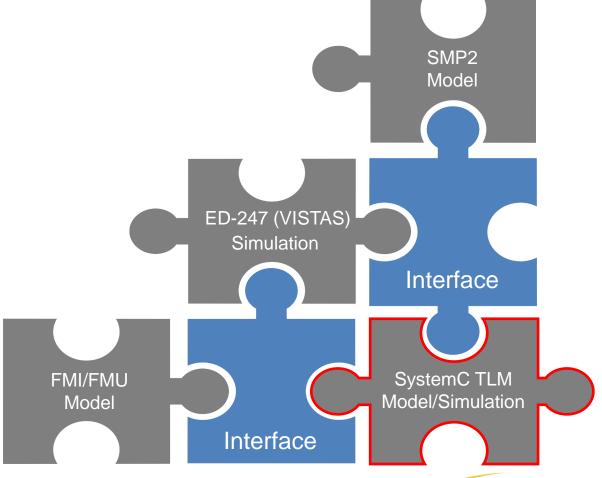
UVM

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Federated Simulation Standard (FSS)

Enabling cross-industry interoperability of simulation frameworks

- Objective: Cross-industry collaboration to improve the interoperability of product and environment simulation
- Approach: Leveraging and connecting existing standards and industry formats
- Introduce standardized interfaces
- Targeting a scalable simulation and modeling ecosystem, covering different levels of the 'OSI stack'







FSS Proposed Working Group & First meeting

- Call for Participation is now open!
 - PWG is open for everyone no Accellera membership required
 - More information and PWG registration:
 https://www.accellera.org/activities/proposed-working-groups
- First in-person meeting **September 25+26, Toulouse, France**
 - Day 1: Discuss industry use cases, requirements, applications
 - Day 2: Organizational aspects incl alignment with other initiatives or organizations
 - More information and event registration: https://evenium.events/8jxrclxh
- Feel free to contact the organization committee for questions and additional information
 - Martin Barnasconi, Mark Burton, Eric Jenn





Next up – SystemC Evolution Day 2023

Mark your calendar

Date: 16 November 2023 (day after DVCon Europe 2023)

Time: 09:30 - 17:30 CET

Location: Holiday Inn Munich City Centre, Hochstrasse 3, 81669 Munich, Germany

- Call for Presentations still open
 - Submit your ideas and contributions for additions and improvements to SystemC and/or its extensions covering TLM, CCI, AMS, Synthesis and/or Verification
 - A contribution can be in the form of a finding, a result, or a proposal, but also a problem experienced that you feel needs attention and discussion in an Accellera and SystemC user-community context
- More information on the event and abstract submission process: https://systemc.org/events/sced2023/





systemc.org

Welcome to the SystemC Community Portal

Your online reference for everything related to SystemC, the language for system-level design, high-level synthesis, modeling and verification.

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Overview
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Downloads

```
#include <systemc>
#include "producer.h"
#include "consumer.h"
class top : public sc_core::sc_module
    fifo fifo_inst{"Fifo1"};
    producer prod_inst{"Producer1"};
    consumer cons_inst{"Consumer1"};
    top(sc core::sc module name name)
    : sc_core::sc_module(name)
      prod inst.out(fifo inst);
      cons_inst.in(fifo_inst);
int sc_main (int, char *[]) {
  top top1("Top1");
  sc_core::sc_start();
  return 0;
```



