DVCon Europe 2025 Modeling Challenge

DVCon Europe 2025

- Deadline scientific papers end June
- (SystemC) Modeling Challenge

DVCCon Europe 2025 (SystemC) Modeling Challenge

Why?

- Get a certificate and present winning solution at DVCon
- Win High-End Laptops etc.
- First submissions eligible to traveling grants

Challenge

- (Low) Power consumption is the new performance since years; weak/no support by SystemC
- Create SystemC model that estimates the power consumption of a small embedded system
  - Input: Inputs of some scenario
  - Output of model: Consumed energy; optional power consumption over time
  - Criteria: accuracy (vs. measurements) and “creative features”

Why Power/Energy?

Energy consumption is key for battery life-time of mobile devices

- SystemC Models can be used during optimization of HW-related SW – Power optimization of FW

Power consumption is relevant for

- Power integrity (IR – Voltage drops)
- Signal integrity (crosstalk)
- Thermal issues (heating, aging)
- Very critical for 3D integration / Chiplets
- SystemC Models can be used during architecture exploration phase

Characterization of SystemC Models is key – circuit level simulation is no option

DVCCon Europe 2025 (SystemC) Modeling Challenge

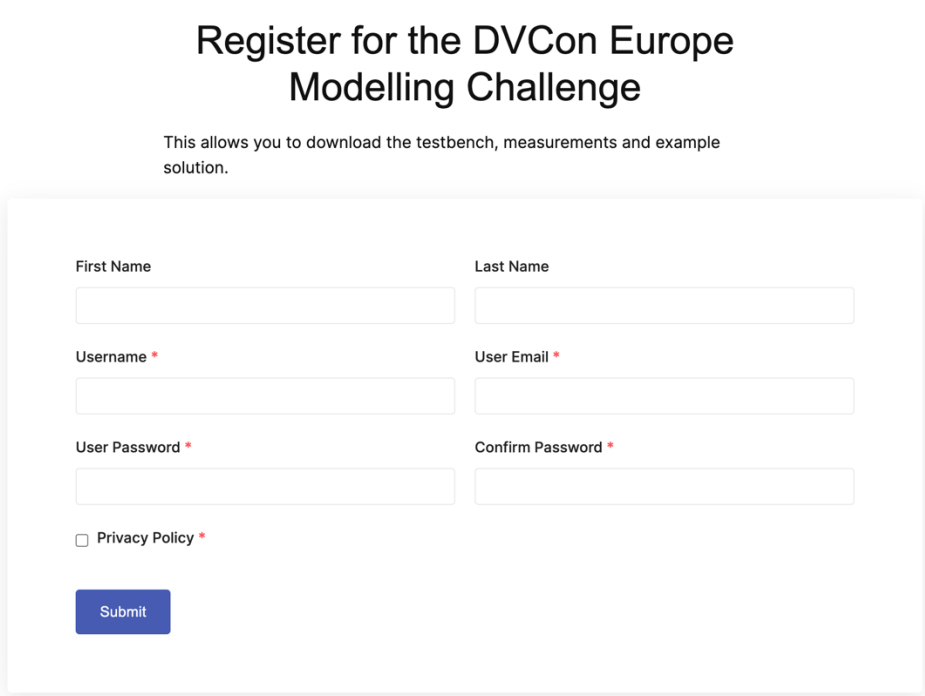
What to do …

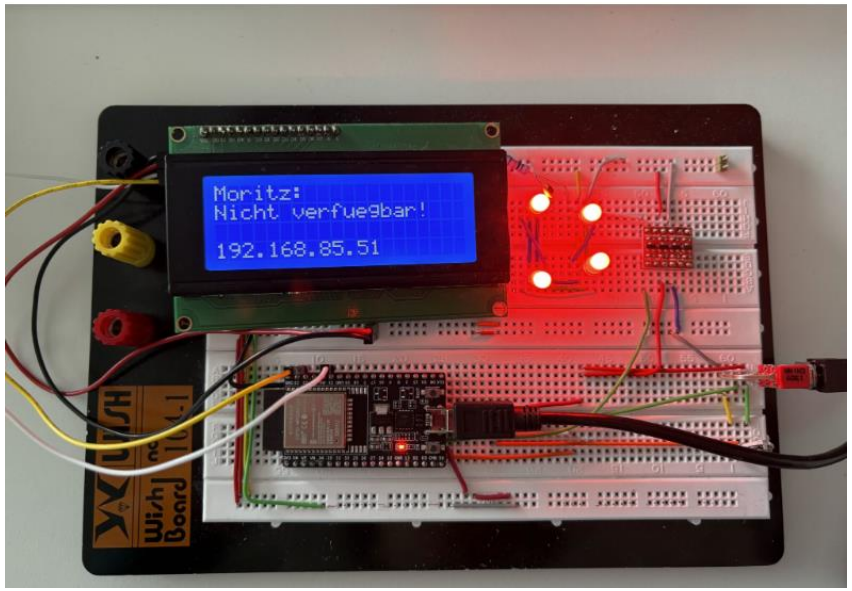
- Register under dvconchallenge.de (Email needed)

- Get
  - Description of embedded system used
  - Dataset with measurements of power
  - Small (and incomplete) test-bench
  - Information and updates

- Join online sessions for Q&A

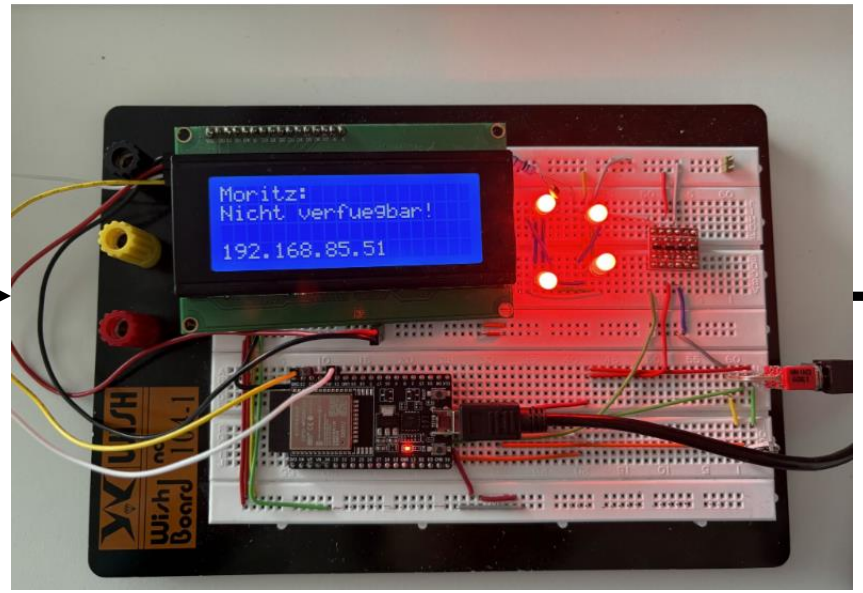
- Submit solutions for review
  - Get feedback
  - updates allowed until October





Measurements and Testbench provided …

Inputs (t)



state (t, input)

power (t)

(Excel table)

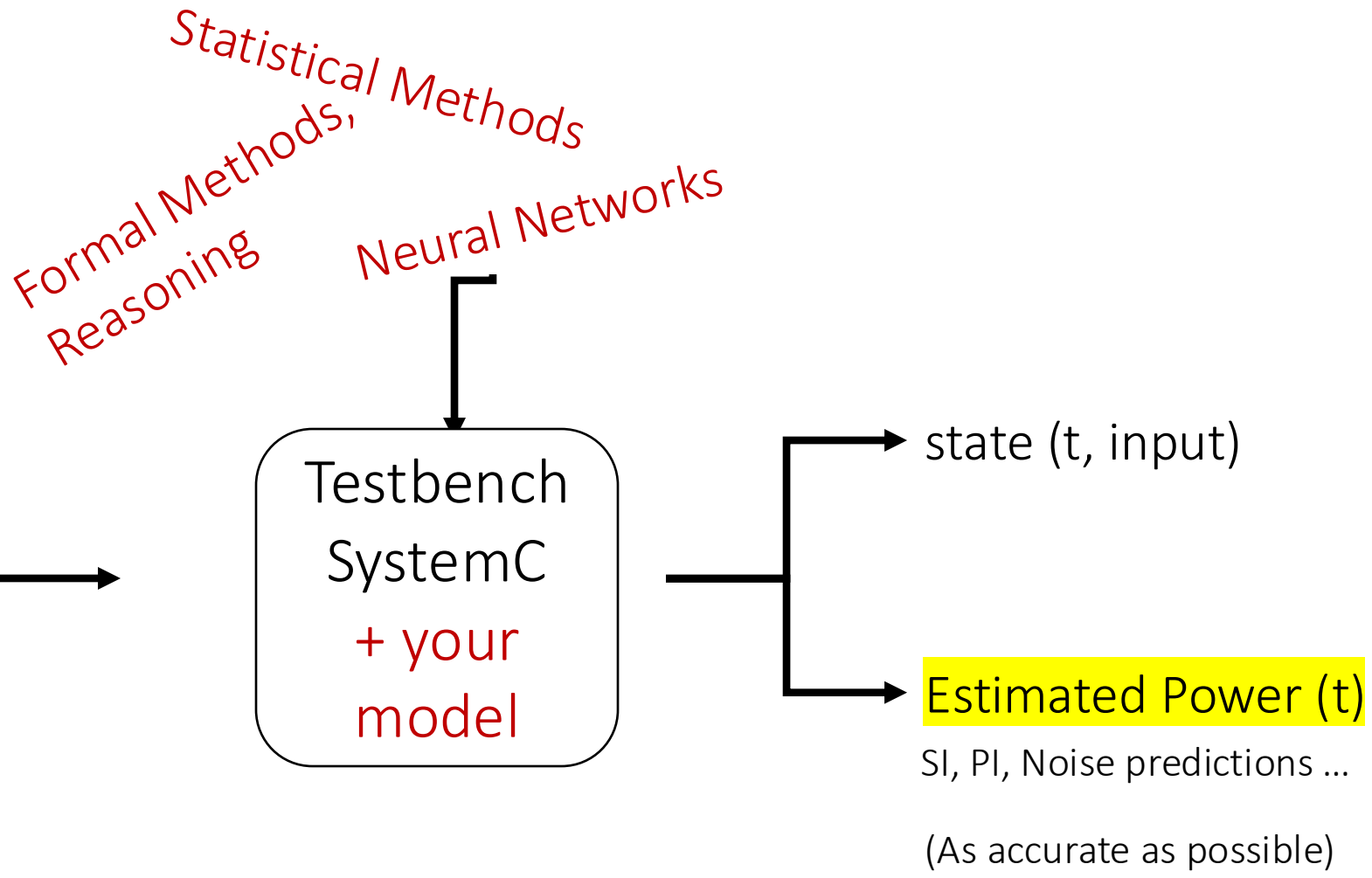
Testbench SystemC + your model

Expected Solution for UNKNOWN Input

Provided data

state (t, input)

power (t)



(As accurate as possible)

Power Estimation at System Level

A Perspective for 3D Integration (shortened)

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Chair of Cyber-Physical Systems

Summary of State of the Art for DVCon Europe 2025 Challenge Participants

DVCon Europe Challenge 2025 deals with power estimation at system level.
Here, we give motivation (3D integration, firmware optimization) and overview of the state of the art.

Power Estimation at System Level

1. 3D integration and power estimation
2. Fundamentals of power estimation
3. Power-aware simulation at system level
4. Summary

3D Integration Challenges (e.g. Wilde 2008; Steinhardt 2019; Bunschwiler 2019)

Heating

- thermo-mechanical issues: thermal expansion, stress
- FEM (Thermal) Simulation of full chip

Crosstalk between layers, vias

- Power- and Signal integrity
- Circuit level simulation with RF/macromodels

System architecture & optimization

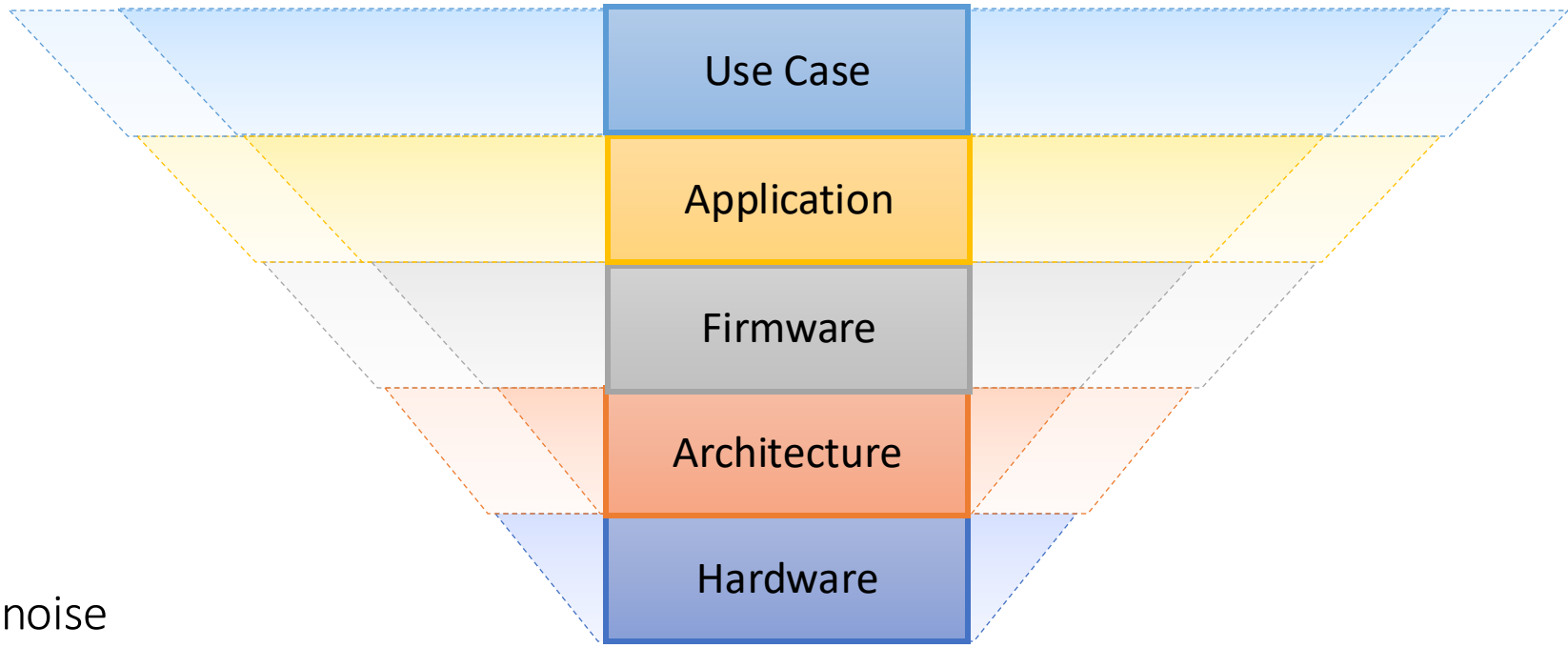
- How much power? noise? current peaks?
- Why? System level optimization of firmware? System partitioning?
- Model based approaches needed!
- Perspective: Link system-level development & circuit level (PVT, SI/PI, Heat, …)

The Power Effect Chain: Inverse Pyramid (Grimm, Moreno 2014)

Cause at use case, system/application level

All levels have major influence on overall power/energy consumption

Effect is current, power, heating, noise



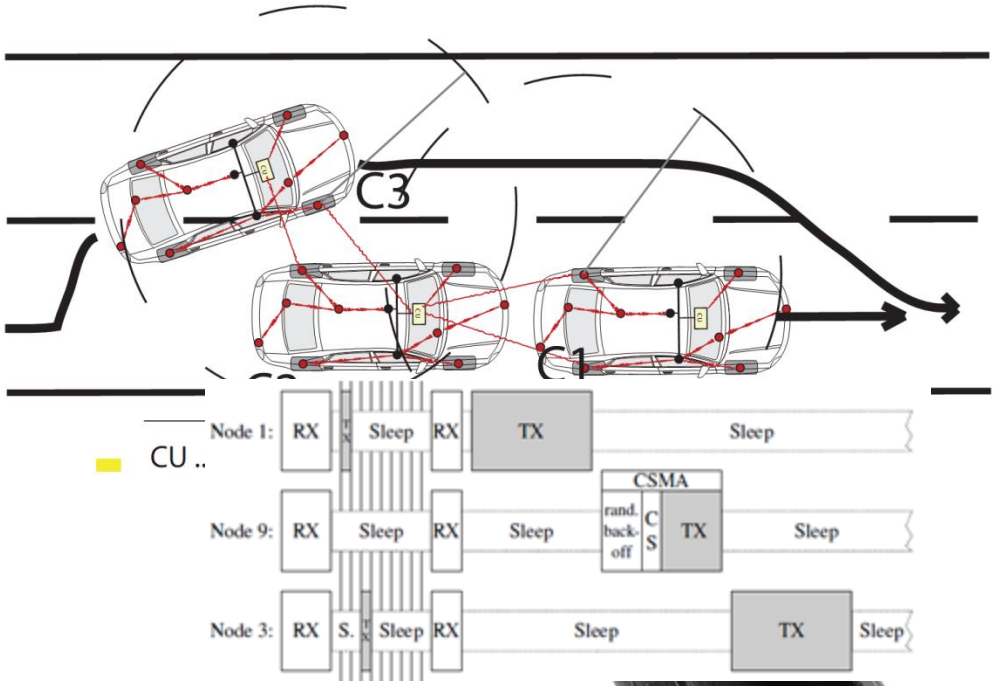
Example: In-Tire TPMS System

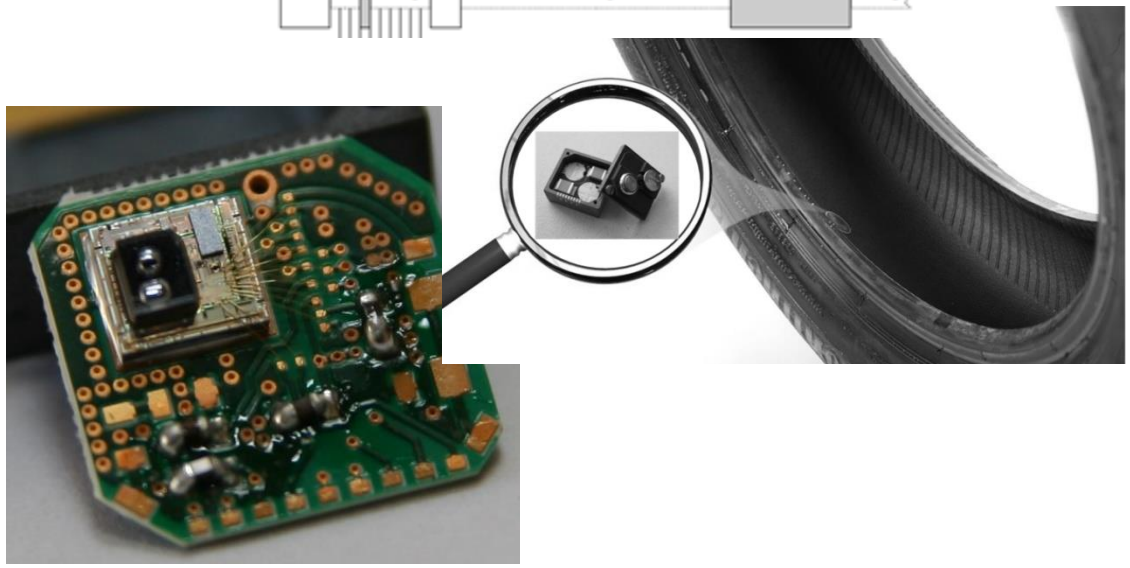
Usage of hardware determines P, I; defined by

- Use case scenario
- Communication protocols
- Architecture

What are relevant worst-case and average currents/power usages?

- Battery lifetime
- Architecture optimization/validation
- (Constraints for estimation crosstalk, heating …)





(3D System; developed with Infineon, Sintef, TU Wien)

Power Estimation at System Level

1. 3D integration and power estimation
2. **Fundamentals of power estimation**
3. Power-aware simulation at system level
4. Outlook

Power: The Physical Hardware View …

Estimation of system power by Excel sheet + guesses based on experience (Lidsk, Rabaey 1996)

Dynamic power (Charging capacity, short circuit)		Static power (Leakage, tunnelling, etc.)
P	$= P_{dyn} +$	P_{stat}
	$= \alpha\, C_L\, V_{DD}^2\, f_{clk} +$	$V_{DD}\, I_{lkg}$
Supply voltage V_{DD} Frequency f_{clk} Switching activity α		Reduce V_{DD} (power down) Temperature → I_{lkg}
PDK; device simulation: C_L		PDK; device simulation I_{lkg}

Less Guessing: Post-Synthesis (Gate Level) Power Aware Simulation

UPF gives information of particular component/system power state as “power intent”

Post-Synthesis Power Aware Simulation gives us

- Number of switching for each logic cell
- Power/Energy information
- Currents information
- Accuracy reported in ranges of +/- 10-20%

Disadvantages

- Often too slow to be useful for use case scenarios with, e.g., 20 sec simulated time
- Hard to consider use case & power management running in SW
- Too late in design flow to be useful for architecture level optimizations
- Limited to digital parts (PLL? Transceiver?)

Power: The System/Software View

Power Management Strategy		Does	Via	Controlled by
FS	Frequency Scaling	Adapts f_{clk}	Clock generator/PLL	Software (OS, Application)
RFTS	Run fast then stop	Power down ($V_{DD} = 0$)	Power gate	
DVFS	Dynamic Voltage Scaling	Adapts f_{clk}, V_{DD}	Clock generator, Power supply	
AVS	Adaptive Voltage Scaling	Adapts f_{clk}, V_{DD} as f(P, T)		

„Power States“ in power management

- Component Power State: (VDD, fclk) for part of system
- System Power State Set of all component‘s power states

NOTE: For power estimation, we use same term, but different meaning!

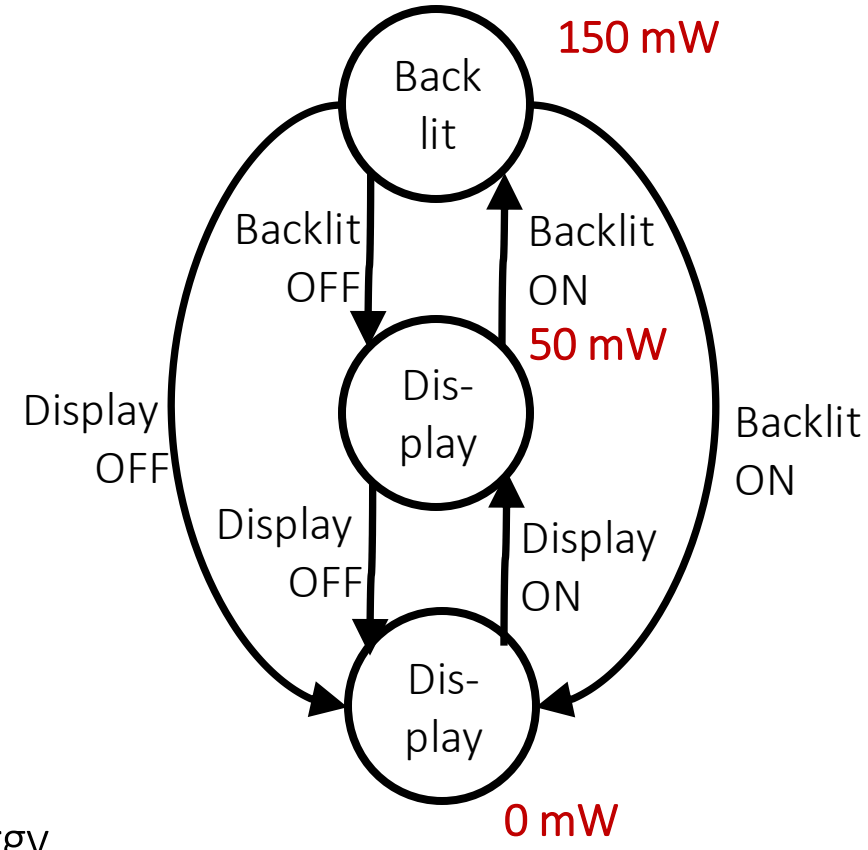
Power Estimation at System Level: Power State Machine (PSM)

Power State Machine (PSM; Benini et al. 1998)

- For arbitrary systems, i.e., notebook:
  - System has power states S = { OFF, DISPLAY, BACLIT}
  - Power state is labeled with average power P, i.e. P(DISPLAY) = 50 mW

- Similar for microelectronic systems (Benini et al. 2000: Memory Access)
  - Power states labeled with power consumption
  - Transitions labeled with energy penalty and delay, i.e., TR(OFF, DISPLAY) = 50 mJ; 20 msec

- Power State **Transition** Machine also labels transitions with energy



Extended PSM (Pan, Grimm 2016; Pan, Grimm 2017)

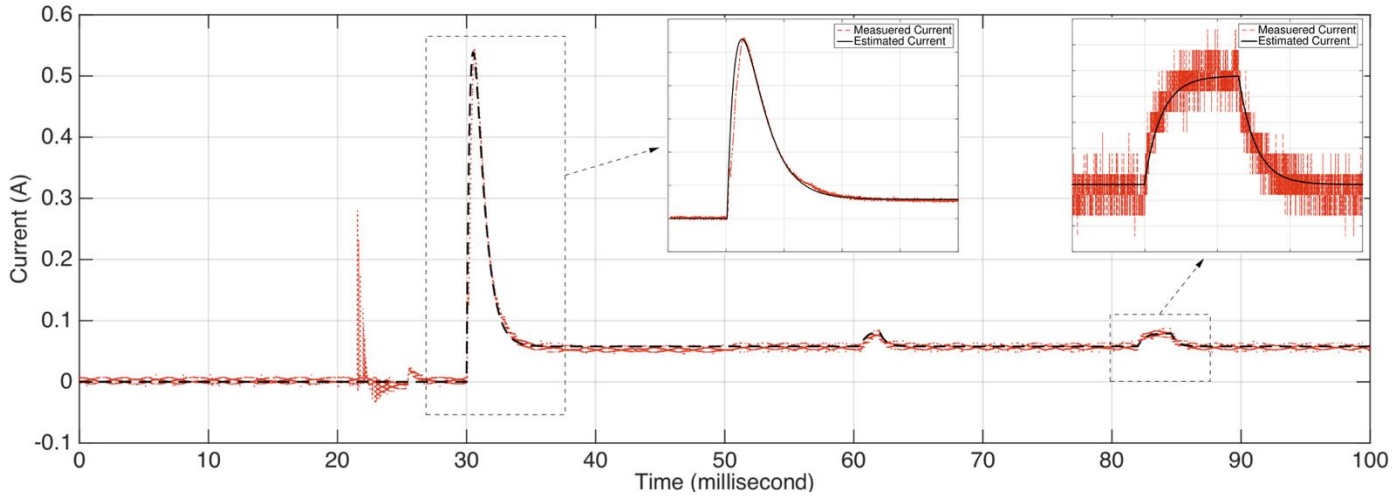
Extended PSM (Pan, Grimm 2016; Pan, Grimm 2017)

Objective: Software/BIOS can (better: must) actively **avoid** critical situations

- Noise on signals (e.g., RF, crosstalk)
- Peak currents that cause SI issues like IR drop, Ground bounce, crosstalk
- *Not for "accurate estimation" – to enable awareness at system level*

Extended PSM

- *PSM States +*
  - *Current & noise model*
- *PSM Transitions +*
  - *Transfer function to allow matching current "overshoots" in transitions by suitable characterization*



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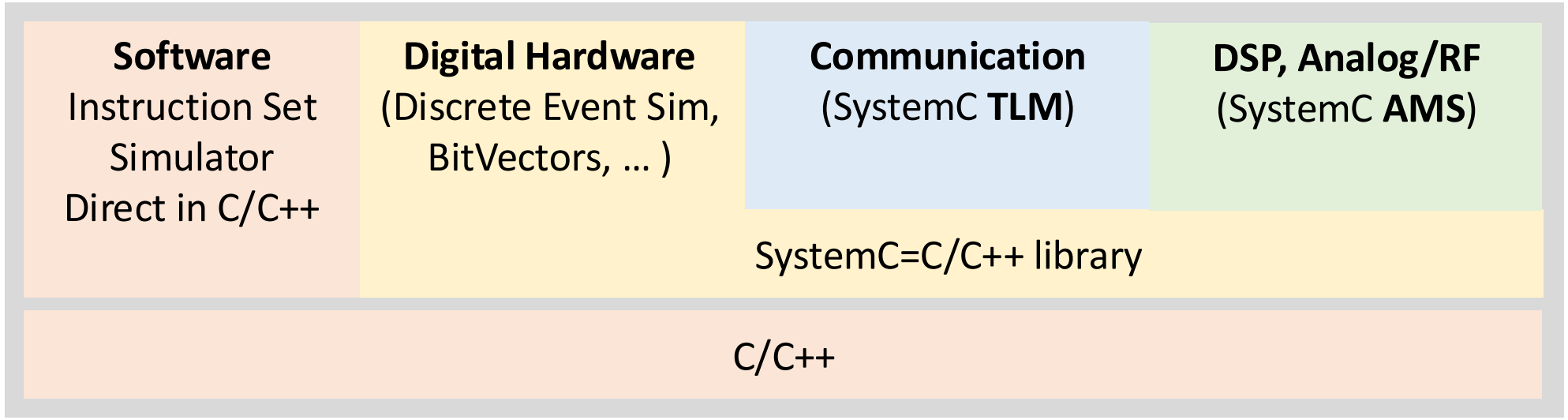
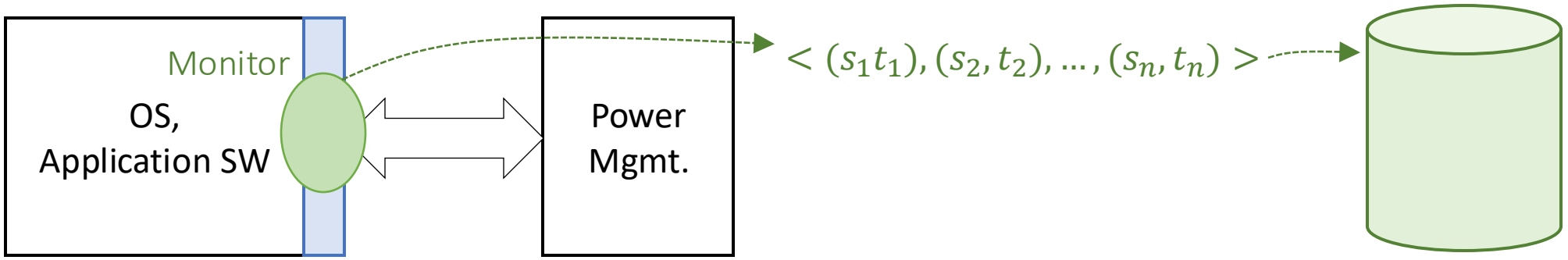
Power Aware System Simulation with SystemC/C/ISS

- Usually **longer simulated time**, e.g., 20 seconds or more
- **Software** is fundamental part of system simulation scenarios
- **SystemC** is IEEE / Accellera Standard targeting (HW/SW) System simulation



Monitoring Transitions for Power-Aware System Simulation



SystemC model with monitors reports changes of power states

- Directly in software
- Monitoring of Busses/Transactions
- …

We save sequence of tuples $(s_i t_i)$ of

- Power state s_i
- Duration t_1

into (compressed) file

(“power trace”)

Energy/Power Estimation with PSTM

Given a power trace $< (s_1 t_1), (s_2, t_2), \ldots, (s_n, t_n) >$

We estimate the energy consumed by

$$E(\mathrm{n}) = \sum_{i=1}^{n} E(Tr(s_{n-1}, s_n)) + P(s_n)\ t_n$$

where

- s_0 is the initial power state
- $E(n)$ is Energy consumed after $n - th$ transition
- $E(Tr(s_{n-1}, s_n))$ is the energy for transition from power state s_{n-1} to s_n
- $P(s_n)$ is the average power consumption in power state s_n
- t_n is the time the system remains in s_n

E(Tr(…)), P(s) by e.g.
- SPICE simulation
- Measurement
- Data sheet
- …

Power Profiling: Closing The Semantic Gap to Software

Power estimation answers the questions:

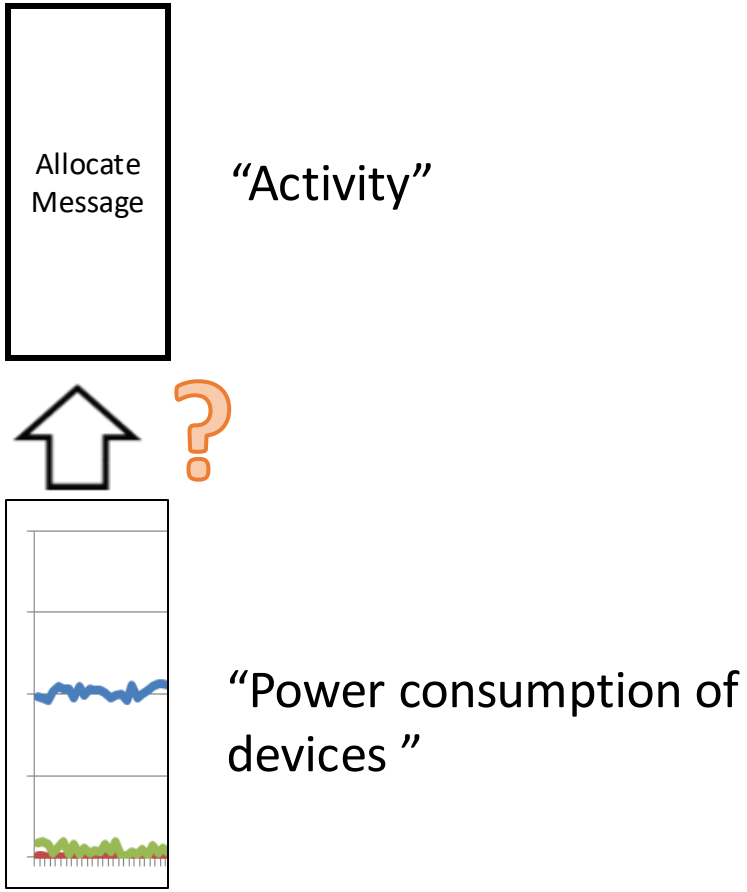
- How much power consumption?
- By which hardware element?

But a SW and system level designer asks the questions

- *Why* was energy consumed? By which (SW-)activity?
- What can we change, optimize in FW, SW?

System/SW/FW Designers need to get insight into

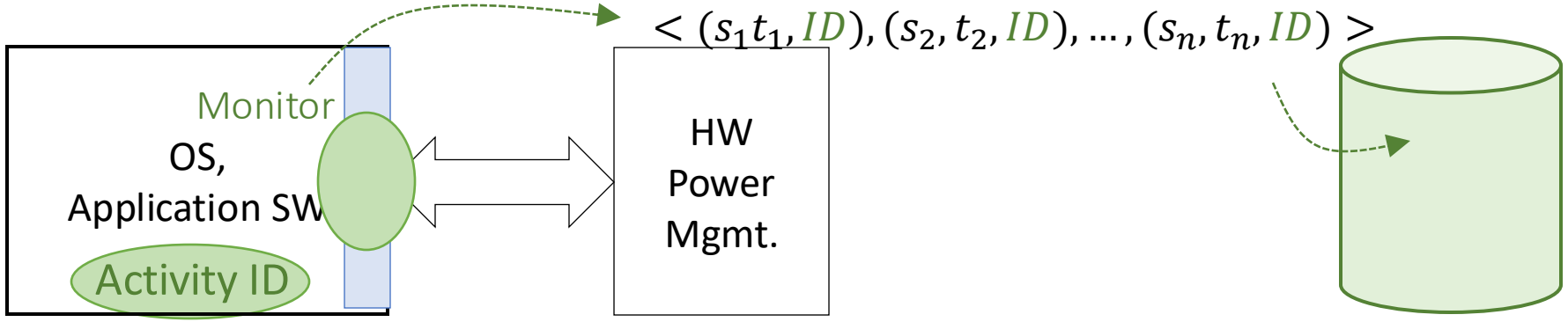
- Functionality that causes consumption of power of component
- Context of it



Power Profiling

Power profiles are *meaningful power consumption data aggregations*

- Power profiling aims to fill the semantic gap
- Assigns power consumption to “activities”
  - *Activities are collections of software processes*
  - *Activities that access power management are instrumented*
  - *Changes in power modes/states are tracked and saved*



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Summary

We presented a modeling & simulation-based approach for power/current-related issues at **system level:**

- PSM = Power / Energy-aware simulation
- Ext. PSM = Noise & peak currents
- Power Profiling links events & consumption with causes in SW activities

Weakness of current EDA – cross-layer flow of information

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